A Method to Implement Low Energy Read Operations, and Single Cycle Write after Read in Subthreshold SRAMs

The Subthreshold Group
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VLSI 6332 Project

Why Operate SRAMs in Subthreshold Supply Voltages?

- $E_{SRAM/cyc} = \frac{1}{2} C_{eff} V_{DD}^2$

  $P_{SRAM} = \frac{1}{2} C_{eff} V_{DD}^2 f_{max}$

- Reducing C_{eff} is costly in terms of design effort

- For low frequency (in kHz) medical circuits, Vdd scaling to subthreshold voltages is very effective

Known Problems in 6T based Subthreshold Bitcells

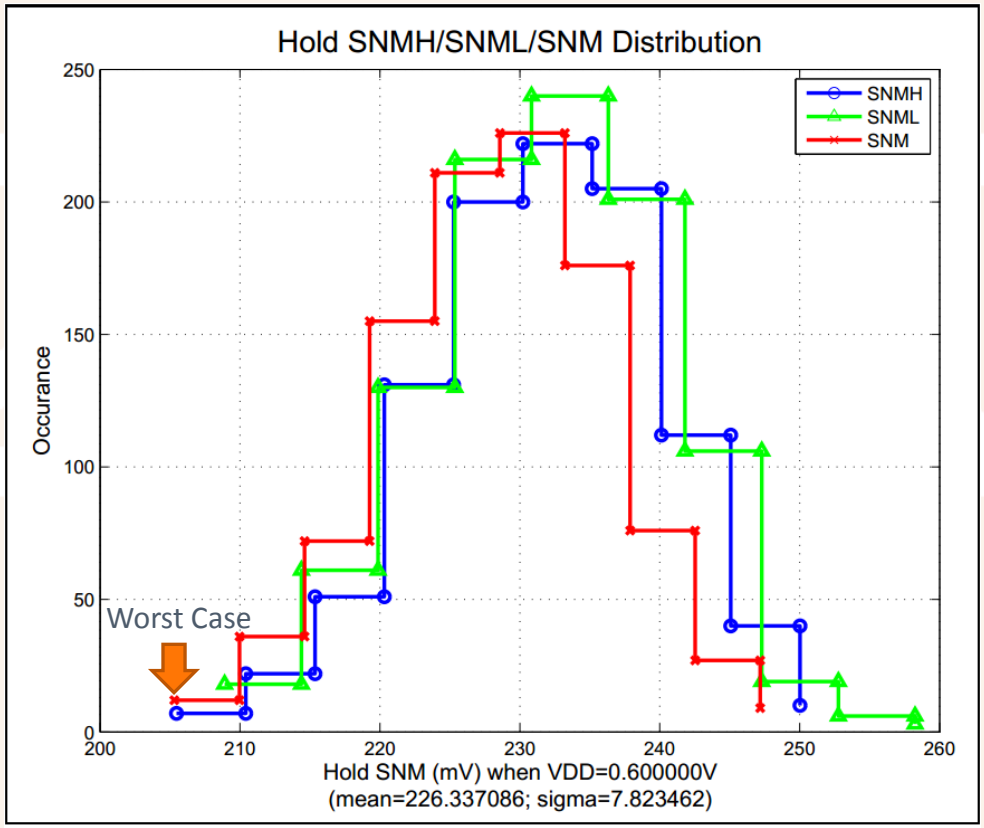
- For 6T based 8T, 9T 10T…
  - Read stress SNM in half selected cells while writing
  - No column muxing is a must
  - Writeback (two cycle write after read) is a must in writing

How to Lower Energy Further in 6T Based Subthreshold SRAMs?

- Possibly voltage scaling?
  - Voltage scaling further? Not a good idea!
  - Vmin is limited by worst case HSNM, VDRV, and so on

Vmin Dependency

- Worst case μ - 3σ hold SNM for 6T based 10T

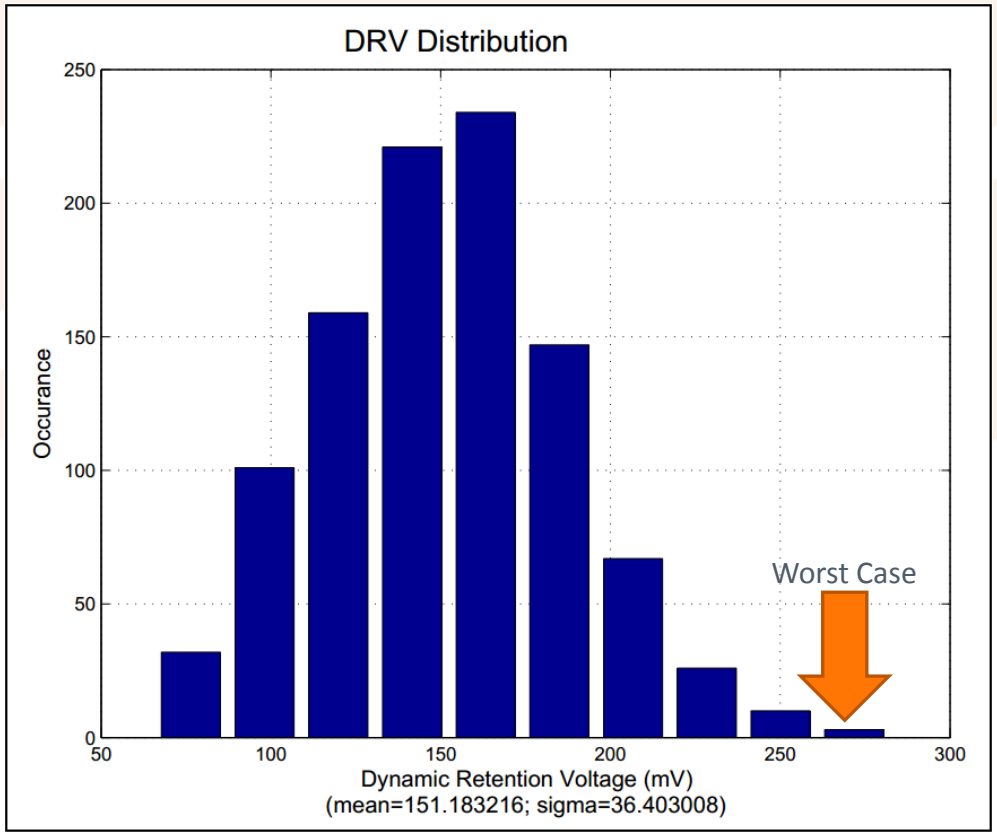


SRAM-HSNM-10T-STn: SRAM-HSNM-10T-STn

MIT 180xlp data provided by James Boley BSN Chip Group @ UVa

Vmin Dependency

- Worst case μ + 3σ data retention voltage (VDRV)



SRAM-DRV-8T: SRAM-DRV-8T

IBM 130nm data provided by James Boley BSN Chip Group @ UVa

Possible Solutions to “How to Lower Energy in 6T Based Subthreshold SRAMs”

- New type of bitcells
- Novel read/write methods
- New SRAM architectures

Earlier Works in SRAM Dynamic Energy/Power Mitigation

Prior Work	Energy/Power Savings
SRAM Read-Assist Scheme, ISOCC, 2011. [6]	21.30%
Low-Energy Disturb Mitigation Scheme IEEE Symposium on VLSI Circuits Digest of Technical Papers , 2011. [7]	32%
Bitline Amplitude Limiting (BAL) Scheme, IEEE Asian Solid-State Circuits Conference on, 2011 [8]	26%
Segmented Virtual Grounding Scheme, ISLPED 2006. [9]	44%
Hierarchical Bitline Scheme ICICDT, 2012. [10]	60%

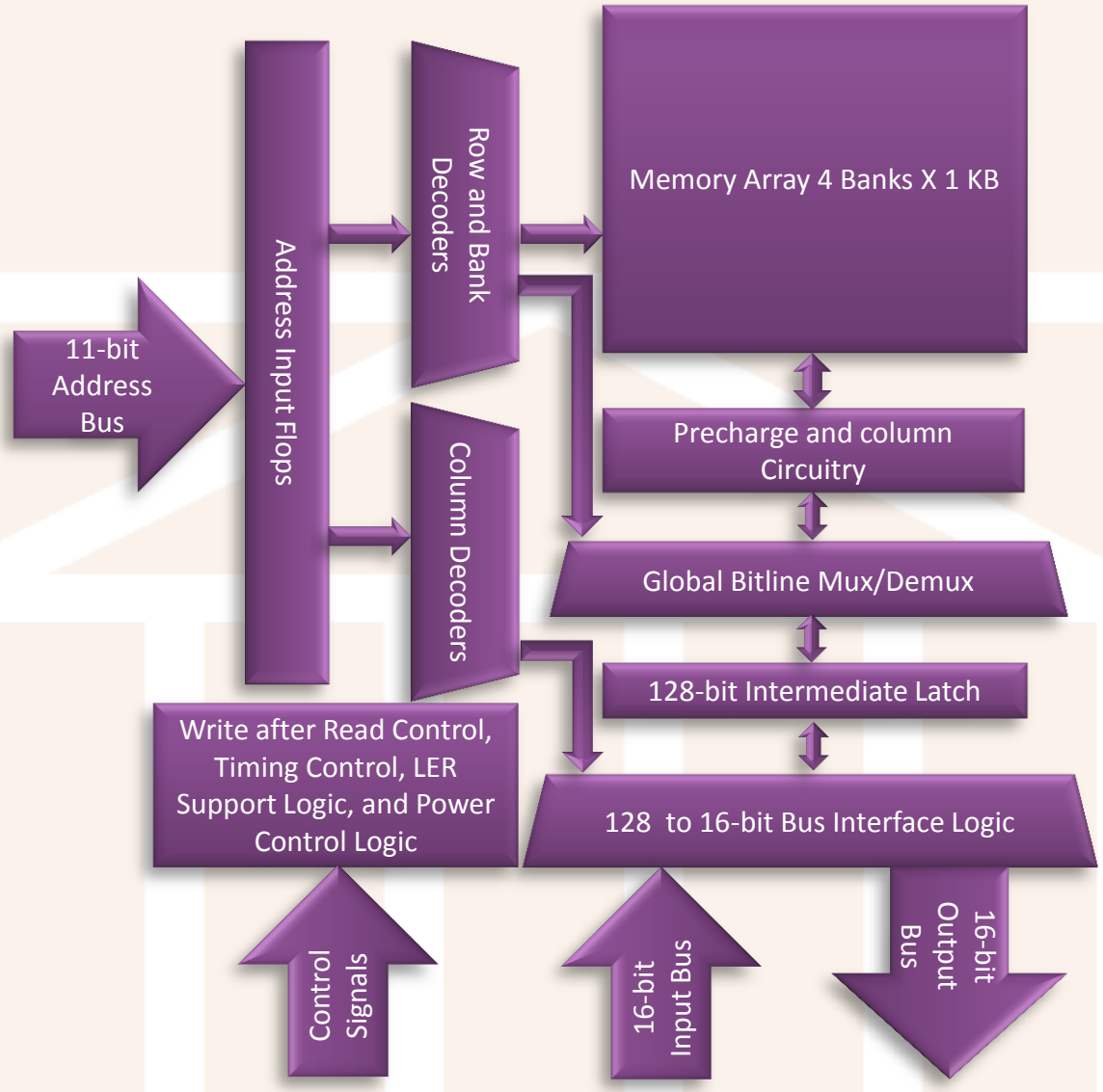
Can We do Better?

- Using RAS-CAS DRAM timing concept in SRAM
- Low Energy Read (LER)?
  - Do not operate decoders, word line drivers
- “N-1” distinct LER operations per one read in N word row
- Auto detection of LER

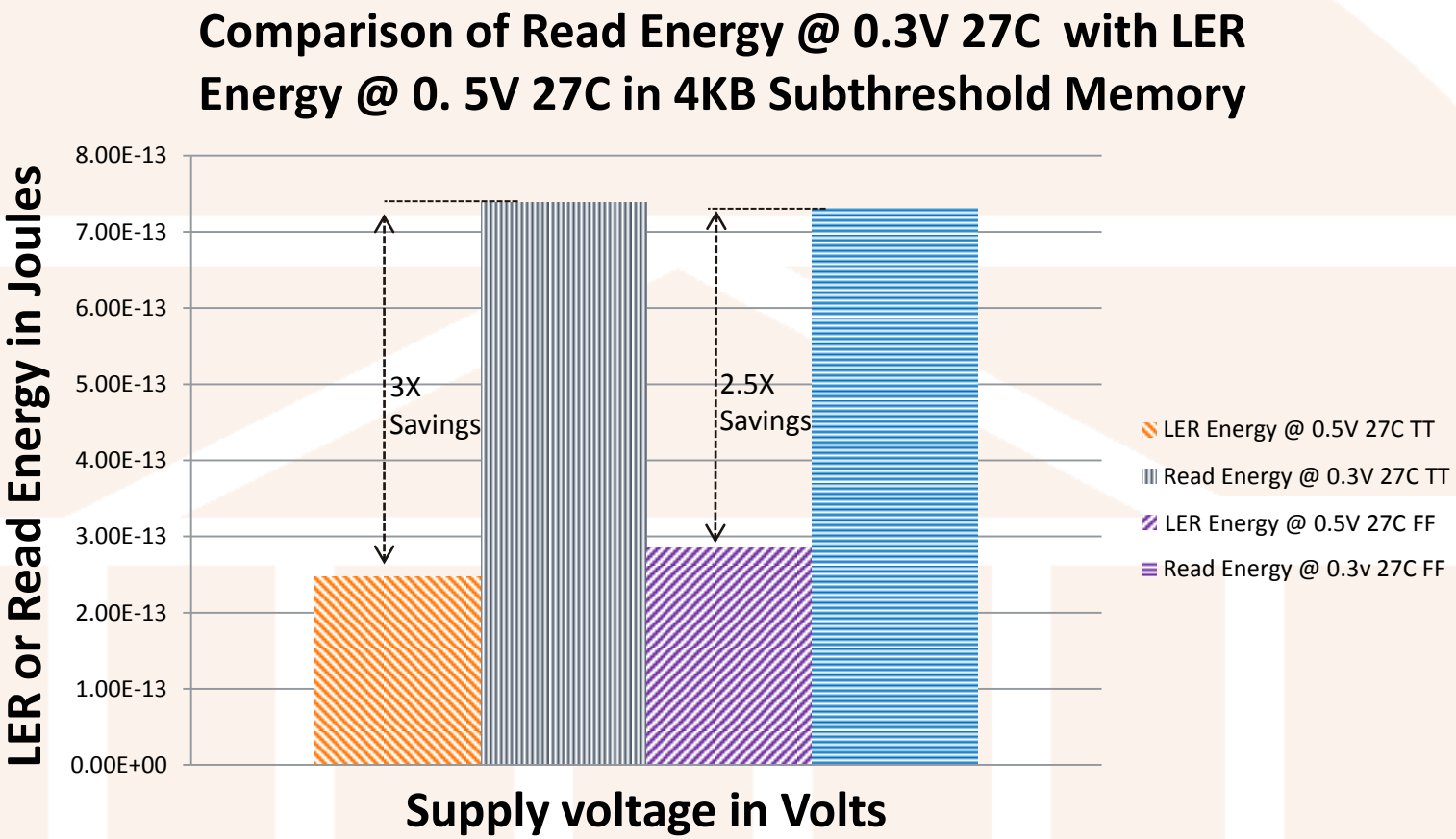
Single Cycle Write after Read(WAR)?

- Earlier approach was two cycle write after read
- Our approach is single cycle write after read
  - Using intermediate latch to latch the read row before write
  - Pulsed read and write word line generation in WAR
  - Controllable WAR margins through external pins

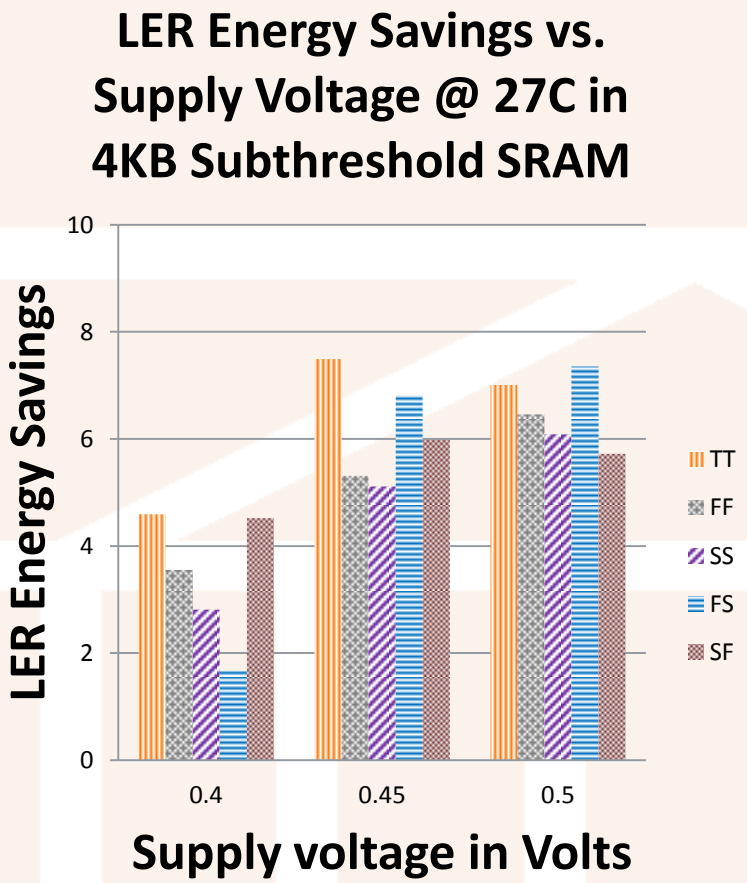
Block Diagram of the 4KB Subthreshold Data Memory

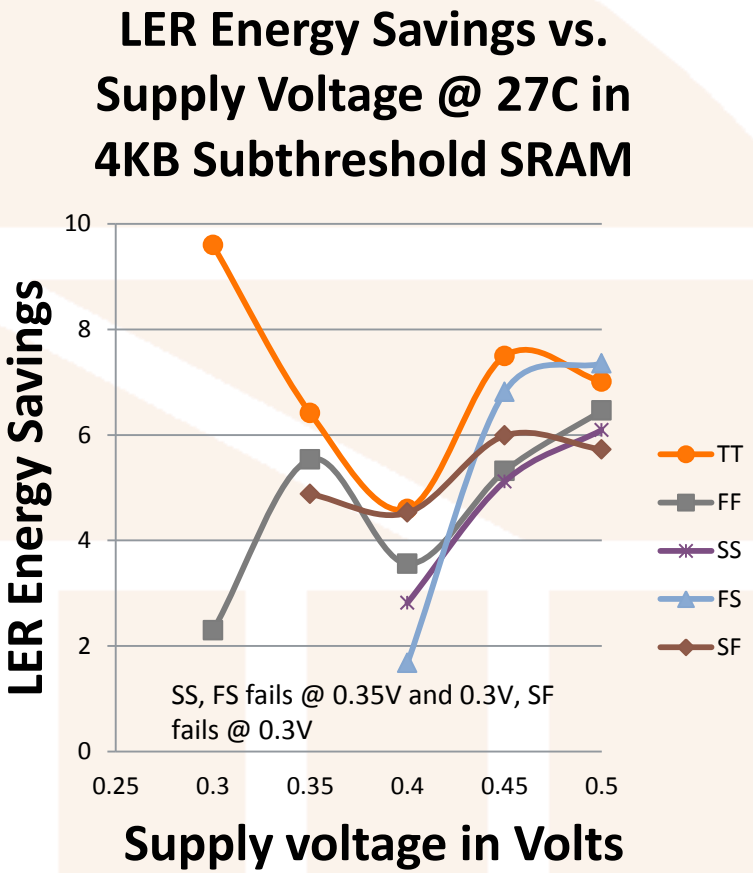


Energy Comparison: Read vs. LER in IBM 130nm Technology



Subthreshold LER Energy Savings Trend in IBM 130nm Technology





Penalty in Our Method

- 7% area
- 3% worst case standby leakage
- 25% worst case WAR energy
- 45% worst case read energy
- Enough room in cycle time with worst case f_{max} of 1.03 MHz for kHz domain operation

Comparison With Prior Works

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Hierarchical Bitline Scheme ICICDT, 2012. [10]	60%
This Work	5.7X @ 0.5V SF 27C, 5.1X @ 0.45 SS 27C, 1.67X @ 0.4 FS 27C

Status of the VLSI 6332 Project

	Tasks	Expected Completion Deadline	Status	Owner
1)	Schematic Implementation of Low Energy Read	9/7/2012	Done	Arijit
2)	Schematic Implementation of Single Cycle Write after Read	9/14/2012	Done	Arijit
3)	Measuring the Energy Saving in Low Energy Mode for in TT, FF, SS, SF and FS corners with 0.5v supply voltage	10/10/2012	Done	Arijit
4)	Checking Design Margins in TT, FF, SS, SF and FS for at least one WR mode	10/10/2012	Done	Arijit
5)	Building Layouts of each new component block	10/10/2012	Done	Arijit
6)	Integrating Layouts to Data Memory	10/30/2012	Done	Jim
7)	Running DRC and LVS over the full SRAM after Integration	10/30/2012	Done	Jim
8)	Extracting Lumped parasitics	11/24/2012	Done	Arijit
9)	Simulate in TT corner with lumped parasitics	12/2/2012	Done	Arijit
10)	Sign off and Tape out on February 2013	February 2013 TBD	To Do	Arijit & Jim
11)	Low Energy Read and Normal Read simulations for energy comparison for 0.5v, 0.45v, 0.4v, 0.35v, 0.3v and superthreshold voltage 0.9v, 1.0V, 1.2V for energy trend comparison	11/14/2012	Done	Arijit

Conclusions

- No need to operate SRAMs in deep subthreshold voltages
- Worst case 5.7X LER energy savings in KHz frequencies @ 0.5V 27C
- Seven distinct LER operations per one read in eight word row
- WAR margins are externally controllable
- Penalty of 7% area, 3% worst case standby leakage, 25% worst case WAR energy, and 45% worst case read energy in design change

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Acknowledgments

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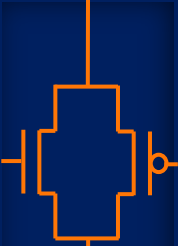
- Professor Mircea Stan, ECE, UVa
- Professor Ben Calhoun, ECE, UVa



Thank You!

Questions?